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| EXAMINER | |
|---|---|
| STOYNOV, STEFAN | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2116 | |

DATE MAILED: 03/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/027,392 | COOPER, BARNES | |
| | Examiner | Art Unit | |
| | Stefan Stoynov | 2116 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *31-35* is/are allowed.

6)☒ Claim(s) *1-3,9-13,19-23,29 and 30* is/are rejected.

7)☒ Claim(s) *4-8,14-18 and 24-28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

### *Claim Rejections - 35 USC § 101*

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 11 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Re claim 11, the specification defines the program or code segments may be stored in a processor readable medium or transmitted by a computer data signal embodied in a carrier wave, or a signal modulated by a carrier, over a transmission medium (paragraph 0013, lines 10-13). Further, examples for processor readable medium include a radio frequency (RF) link (paragraph 0013, line 17) and for the transmission medium – air and RF links (paragraph 0013, line 19). The media listed above is intangible. Therefore the "machine usable medium having computer program code embedded therein" is incapable of being touched or perceived absent the tangible medium through which it is conveyed thus rendering the claim non-statutory.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-3, 9-13, 19-23, 29, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Sun.

Re claims 1, Nakamura discloses a method comprising:

loading the SMI timer with a timer value (column 8, lines 26-28) based on the processor state (column 17, lines 65-67, column 18, lines 1-6, lines 18-21), the timer value being one of a first value and a second value (FIG. 11C, T1 and T2);

Nakamura also discloses the processor having an operational state (column 6, lines 1-4) and a low power state (column 6, lines 7-10).

Nakamura fails to disclose determining the processor state upon expiration of a system management interrupt (SMI) timer and transitioning the processor to one of the operational state and the low power state according to the processor state.

Sun teaches a CPU receiving a SMI signal from a timer upon which a SMI handler is invoked (column 3, lines 53-55). Sun does not specifically teach the SMI signal being generated upon expiration of the timer. However, Sun teaches the timer supplying the SMI signal to the CPU periodically, being activated after a given sampling period (column 3, lines 14-18, column 3, lines 27-29) thus the SMI signal is being generated periodically upon expiration of the timer. Sun further teaches the SMI handler (invoked by the SMI) determining the usage state for each device and based on this determination adapting the power management parameters for the device (transitioning or not the device to reduced power) (column 3, lines 53-67). In Sun, the described method is used to continually adapt the computer's power distribution to the current

usage parameters. This avoids active devices being powered down and at the same time conserving energy by reducing power to idle devices (column 2, lines 10-14). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the device usage state determination and power transitioning method by means of SIM signal generated upon expiration of a timer, as suggested by Sun with the method disclosed by Nakamura in order to implement determining a processor state of a processor upon expiration of a system management interrupt (SMI) timer and transitioning the processor to one of operational state and a low power state according to the processor state.

Re claim 11, Sun further teaches a computer program product comprising:

a machine usable medium having computer program code embedded therein (column 3, lines 12-18, lines 53-55), the computer program product having:

computer readable program code to determine a processor state of a processor (column 3, lines 53-67) upon expiration of a system management interrupt (SMI) timer (column 3, lines 14-18, column 3, lines 27-29)

transitioning the processor to one of the operational state and the low power state according to the processor state (column 2, lines 10 and 11, column 3, lines 53-67)

Re claim 11, Nakamura further discloses:

the processor state being one of an operational state (column 6, lines 1-4) and a low power state (column 6, lines 7-10);

computer readable program code to load the SMI timer with a timer value (column 8, lines 26-28) based on the processor state (column 17, lines 65-67, column

18, lines 1-6, lines 18-21), the timer value being one of a first value and a second value (FIG. 11C, T1 and T2);

Re claim 21, Nakamura further discloses a system comprising:

a processor (FIG. 1, 11);

a memory coupled to the processor (FIG. 1) to store the throttling emulator (column 7, lines 28-32, lines 38-42), the throttling emulator when executed, causing the processor to:

load the SMI timer with a timer value (column 8, lines 26-28) based on the processor state (column 17, lines 65-67, column 18, lines 1-6, lines 18-21), the timer value being one of a first value and a second value (FIG. 11C, T1 and T2);

Re claim 21, Sun further teaches:

determine a processor state of a processor (column 3, lines 53-67) upon expiration of a system management interrupt (SMI) timer (column 3, lines 14-18, column 3, lines 27-29)

transition the processor to one of the operational state and the low power state according to the processor state (column 2, lines 10 and 11, column 3, lines 53-67)

Re claims 2, 12, and 22, Nakamura further discloses the method, computer program product, and system comprising:

loading the SMI timer with first value (column 17, line 67, column 18, lines 1-6, and FIG. 11C, T2) if the processor state is the operational state (FIG. 11B); and

loading the SMI timer with the second value (column 18, lines 18-30 and FIG. 11C, T1) if the processor sate is the low power state (FIG. 11B).

Re claims 3, 13, and 23 Nakamura further discloses the method, computer program product, and system comprising:

transitioning the processor to the operational state if the processor state is the low power state (FIG. 11B); and

transitioning the processor to the reduced power state if the processor is operational state (FIG. 11B).

Re claims 9, 19, and 29, Nakamura further discloses the method, computer program product, and system comprising:

transitioning the processor to a sleep state (column 6, lines 34-39 and FIG. 2).

Re claims 10, 20, and 30, Nakamura further discloses the method, computer program product, and system comprising:

loading the SMI timer in a chipset (column 7, lines 10-13, gate array defined as chip in Microsoft Computer Dictionary, Fifth Edition).

***Allowable Subject Matter***

Claims 4-8, 14-18, and 24-28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 31-35 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Re claims 4, 14, and 24, the prior art fails to disclose or suggest "disabling the SMI timer if throttling is disabled; and enabling the SMI timer is throttling is enabled".

Re claims 5, 15, and 25, the prior art fails to disclose or suggest "updating the throttling state if the access is a write; and returning the throttling state if the access is a read".

Re claim 31, the prior art fails to disclose or suggest "in response to receiving an interrupt, determining whether throttling is enabled; and if throttling is enabled, loading a periodic timer with a first timer value".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stefan Stoynov whose telephone number is (571) 272-4236. The examiner can normally be reached between 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

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